

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A failure analysis system of a logic LSI having software incorporated therein, comprising:

a function to record [[the]] a test terminal signal information of [[said]] a testing logic LSI as a target of analysis in synchronization with a clock signal;

a function to reproduce said test recorded terminal signal information in synchronization with the clock signal; [[and]]

a function to compare said reproduced terminal signal information with [[the]] a reference terminal signal information of a normal logic LSI; and

a trace data map of a condition change in a register data and a RAM data for a specific period of time.

Claim 2 (Currently Amended): A failure analysis system of a logic LSI having software incorporated therein, comprising:

a function to record [[the]] a test terminal signal information of [[the]] a testing logic LSI as a target of analysis in synchronization with a clock signal;

a function to record [[the]] a reference terminal signal information of a normal

logic LSI in synchronization with a clock signal; [[and]]

a function to compare said recorded test terminal signal information of the logic LSI as the target of analysis with said recorded reference terminal signal information of the normal logic LSI; and

a function to generate a trace difference map of a trace data map of the testing logic LSI and a trace data map of the normal logic LSI.

Claim 3 (Currently Amended): A failure analysis system of a logic LSI having software incorporated therein, comprising:

a function to record [[the]] a test terminal signal information of [[the]] a testing logic LSI as a target of analysis in synchronization with a clock signal;

a function to reproduce said test recorded terminal signal information in synchronization with a clock signal; [[and]]

a function to compare said reproduced test terminal signal information of the logic LSI as the target of analysis with [[the]] a reference terminal signal information of an emulator of a logic LSI; and

a function to vary a reproduction speed of the test terminal signal information.

Claim 4 (Currently Amended): A failure analysis system of a logic LSI having software incorporated therein, comprising:

a function to record [[the]] a test terminal signal information of [[the]] a testing

logic LSI as a target of analysis in synchronization with a clock signal; [[and]]
a function to compare said recorded test terminal signal information of ~~the logic~~
~~LSI as the target of analysis~~ with [[the]] a reference terminal signal information of [[the]]
an emulator of [[the]] a logic LSI; and
a function to save conditions of a RAM and a register before generation of a
defect, and to resume the conditions of the RAM and the register using the conditions
from before generation of the defect.

Claims 5-6 (Canceled)

Claim 7 (Currently Amended): A failure analysis system of a logic LSI according to
claim [[1]] 2, wherein said failure analysis system further has a function to generate a
plurality of [[said]] trace difference maps by generating a plurality of defects and to
obtain [[the]] an average and [[the]] a data spread of [[the]] a difference by a statistical
work.

Claim 8 (Canceled)

Claim 9 (Currently Amended): A failure analysis system of a logic LSI according to
claim 1, wherein said failure analysis system further has a function to record [[the]] a
command trace data of a CPU in synchronization with said reference terminal signal

information.

Claim 10 (Canceled)

Claim 11 (Currently Amended): A failure analysis system of a logic LSI according to claim 1, wherein said failure analysis system further has a function to connect comparative signals of a plurality of logic LSIs to multiinput OR terminals and to analyze a plurality of logic LSIs at the same time.

Claim 12 (Currently Amended): A failure analysis system of a logic LSI according to claim 1, wherein said test terminal signal information also includes [[the]] an analog signal information.

Claim 13 (Currently Amended): A failure analysis system of a logic LSI according to claim 12, wherein said failure analysis system further has a function to obtain in advance analog/digital difference properties of the testing logic LSI ~~as the analysis target~~ and the normal logic LSI, or digital/analog difference properties thereof and to correct an analog conversion property.

Claim 14 (Currently Amended): A failure analysis system of a logic LSI according to claim 12, wherein said testing logic LSI has an on-chip debugger mounted thereon.

Claim 15 (Currently Amended): A failure analysis system of a logic LSI according to claim 1, wherein said failure analysis system further has layered software.

Claim 16 (Currently Amended): A failure analysis system of a logic LSI according to claim 1, wherein the analysis target of analysis is a system having a logic LSI mounted thereon.

Claim 17 (Currently Amended): A failure analysis method of a logic LSI having software incorporated therein comprising:

~~means to record the recording a test terminal signal information of [[said]] a testing logic LSI as a target of analysis in synchronization with a clock signal;~~

~~means to reproduce said reproducing the recorded test terminal signal information in synchronization with the clock signal; [[and]]~~

~~means to compare said comparing the reproduced test terminal signal information with [[the]] a reference terminal signal information of a normal logic LSI; and~~

~~producing a trace data map of a condition change in a register data and a RAM data for a specific period of time.~~

Claim 18 (Currently Amended): A failure analysis method of a logic LSI having software incorporated therein comprising:

~~means to record the recording a test terminal signal information of [[the]] a~~

testing logic LSI as a target of analysis in synchronization with a clock signal;
~~means to record the recording a reference terminal signal information of a~~
normal logic LSI in synchronization with a clock signal; [[and]]
~~means to compare said comparing the recorded test terminal signal information~~
~~of the logic LSI as the target of analysis with [[said]] recorded reference terminal signal~~
~~information of the normal logic LSI; and~~
generating a trace difference map of a trace data map of the testing logic LSI
and a trace data map of the normal logic LSI.

Claim 19 (Currently Amended): A failure analysis method of a logic LSI having software incorporated therein comprising:

~~means to record the recording a test terminal signal information of [[the]] a~~
testing logic LSI as a target of analysis in synchronization with a clock signal;
~~means to reproduce said reproducing the recorded test terminal signal~~
information in synchronization with the clock signal; [[and]]
~~means to compare said comparing the reproduced test terminal signal~~
information of the logic LSI as the target of analysis with [[the]] a reference terminal
signal information of an emulator of a logic LSI; and
varying a reproduction speed of the test terminal signal information.

Claim 20 (Currently Amended): A failure analysis method of a logic LSI having software incorporated therein comprising:

~~means to record the recording a test terminal signal information of [[the]] a testing logic LSI as a target of analysis in synchronization with a clock signal; [[and]] means to compare said comparing the recorded test terminal signal information of the logic LSI as the target of analysis with [[the]] a reference terminal signal information of [[the]] an emulator of [[the]] a logic LSI;~~

saving conditions of a RAM and a register before generation of a defect; and resuming the conditions of the RAM and the register using the conditions from before generation of the defect.

Claims 21 – 22 (Canceled)

Claim 23 (Currently Amended): A failure analysis method of a logic LSI according to claim [[17]] 18, wherein said failure analysis method further has means to generate comprising:

generating a plurality of [[said]] trace difference maps by generating a plurality of defects; and to obtain the obtaining an average and [[the]] a data spread of [[the]] a difference by a statistical work.

Claim 24 (Canceled)

Claim 25 (Currently Amended): A failure analysis method of a logic LSI according to claim 17, wherein said failure analysis method further has means to record the comprising recording a command trace data of a CPU in synchronization with [[said]] the reference terminal signal information.

Claim 26 (Canceled)

Claim 27 (Currently Amended): A failure analysis method of a logic LSI according to claim 17, wherein said failure analysis method further has means to connect comprising connecting a plurality of comparative signals of a plurality of logic LSIs to a plurality of multiinput OR terminals; and
to analyze a analyzing the plurality of logic LSIs at the same time.

Claim 28 (Currently Amended): A failure analysis method of a logic LSI according to claim 17, wherein [[said]] the test terminal signal information also includes [[the]] an analog signal information.

Claim 29 (Currently Amended): A failure analysis method of a logic LSI according to claim 28, wherein said failure analysis method further has means to obtain comprising:

obtaining in advance analog/digital difference properties of the testing logic LSI as the analysis target and the normal logic LSI, or digital/analog difference properties thereof; and
to correct correcting an analog conversion property.

Claim 30 (Currently Amended): A failure analysis method of a logic LSI according to claim 28, wherein [[said]] the testing logic LSI has an on-chip debugger mounted thereon.

Claim 31 (Currently Amended): A failure analysis method of a logic LSI according to claim 17, wherein the analysis target of analysis is a system having a logic LSI mounted thereon.